REV	Description	DATE	BY
C	1. Improved layout for the USB PHY. 2. Removed unused parts from the design. 3. Added current measurement function to the TWL4030. 4. Added filter caps to the VBUS rail input and output. 5.Changed U9 & U11 package to the QFN..	8/14/08	GC
C1	1. Added J12 and J13 to provide access to the RGB TTL signals on the LCD. 2. Added 5 filter caps. 3. Moved the USB Host port from Port1 to Port2. 4. Deleted R1. 5. Added 10K pulldown to USB reset signal. 6. Added 10K pulldown resistors as ID function to determine board type by reading these pins. 7. Added series resistor, R53, in the CLK line of the HSUSB clock line. May be removed after testing.	10/1/08	GC
C2	1. Moved the McBSP3_DX signal to pin AB26. 2. Moved the McBSP3_DR signal to pin AB25. 3. Moved the McBSP3_CLKX signal to pin AD25. 4. Changes were to allow access to three PWM signals from OMAP3530.	12/16/08	GC
C3	1. Added series resistor to BKBAT. 2. Added TP to BKBAT to allow access for battery. 3. Added a 47pf CAP and 3.3uH inductor to the S-Video feedback resistors.	2/11/2009	GC
C3A	1. Switched to TPS65950 based on the availability of the parts. 2. Made the batttery an installed component. Removed parallell resistor.	4/21/2009	GC
C3B	1. Corrected J4 and J5 symbol for the RGB interface.No electrical changes were made. 2. Removed battery as an installed component due to availability issues.	4/30/2009	GC
C4	1. Added C141, 22uF in parallell with C97. 2. Added option to allow the USB PHY and CLKOUT to be powered from the VIO_1V8 rail or the VAUX2 rail from the TPS65950. Default is VIO_1V8 rail. 3. Changed 1.8V filter CAP on USB PHY to 22uf. 4. Made R113 a DNI and installed R112.	10/5/2009	GC
C4A	1. Made R67 an installed inductor and made R68 a DNI. Switched to LDO powered EHCI USB Phy.	11/5/2009	GC
C4B	1. Made R112 as a install and a value of 510 ohms. 2. Made R113 a DNI.	12/15/2009	GC

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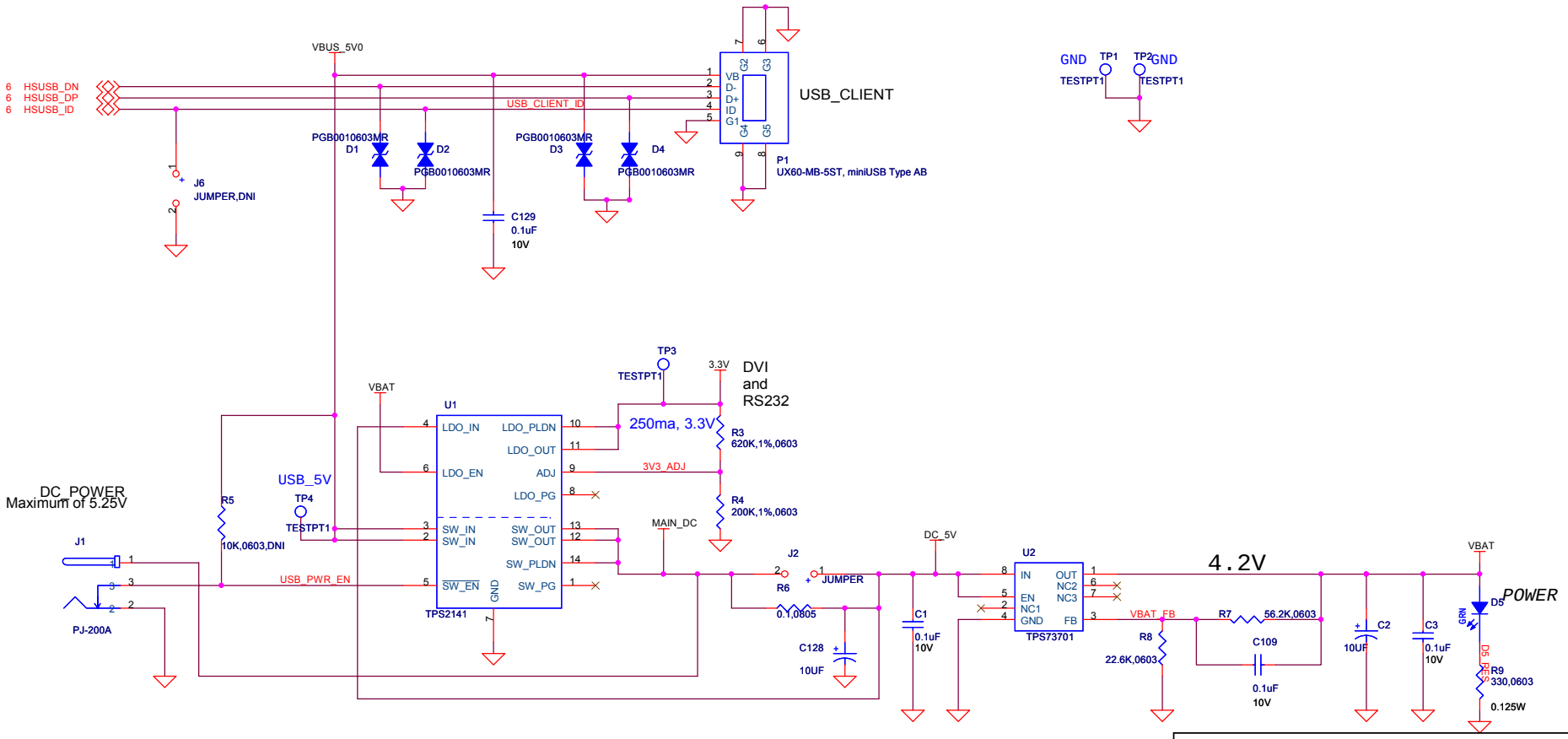

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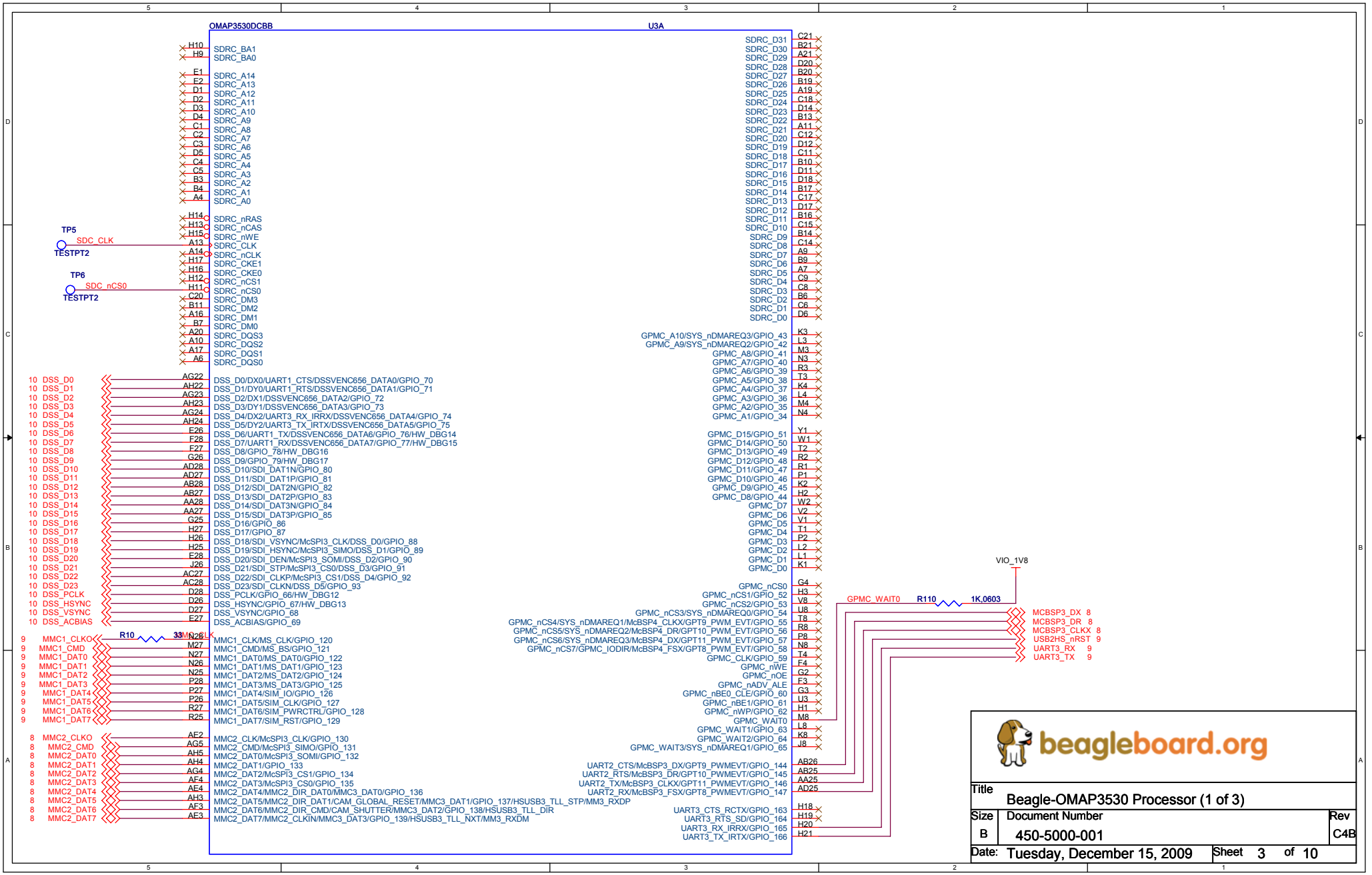
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U3A
SDRC_BA1
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SDRC_A13
SDRC_A12
SDRC_A11
SDRC_A10
SDRC_A9
SDRC_A8
SDRC_A7
SDRC_A6
SDRC_A5
SDRC_A4
SDRC_A3
SDRC_A2
SDRC_A1
SDRC_A0
SDRC_nRAS
SDRC_nCAS
SDRC_nWE
SDRC_CLK
SDRC_nCLK
SDRC_CKE1
SDRC_CKE0
SDRC_nCS1
SDRC_nCS0
SDRC_DM3
SDRC_DM2
SDRC_DM1
SDRC_DM0
SDRC_DQS3
SDRC_DQS2
SDRC_DQS1
SDRC_DQS0
TP5
SDC_CLK
TESTPT2
TP6
SDC_nCS0
TESTPT2
DSS_D0/DX0/UART1_CTS/DSSVENC656_DATA0/GPIO_70
DSS_D1/DY0/UART1_RTS/DSSVENC656_DATA1/GPIO_71
DSS_D2/DX1/DSSVENC656_DATA2/GPIO_72
DSS_D3/DY1/DSSVENC656_DATA3/GPIO_73
DSS_D4/DX2/UART3_RX_IRRX/DSSVENC656_DATA4/GPIO_74
DSS_D5/DY2/UART3_TX_IRTX/DSSVENC656_DATA5/GPIO_75
DSS_D6/UART1_TX/DSSVENC656_DATA6/GPIO_76/HW_DBG14
DSS_D7/UART1_RX/DSSVENC656_DATA7/GPIO_77/HW_DBG15
DSS_D8/GPIO_78/HW_DBG16
DSS_D9/GPIO_79/HW_DBG17
DSS_D10/SDI_DAT1N/GPIO_80
DSS_D11/SDI_DAT1P/GPIO_81
DSS_D12/SDI_DAT2N/GPIO_82
DSS_D13/SDI_DAT2P/GPIO_83
DSS_D14/SDI_DAT3N/GPIO_84
DSS_D15/SDI_DAT3P/GPIO_85
DSS_D16/GPIO_86
DSS_D17/GPIO_87
DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88
DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89
DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_D2/GPIO_90
DSS_D21/SDI_STP/McSPI3_CS0/DSS_D3/GPIO_91
DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92
DSS_D23/SDI_CLKN/DSS_D5/GPIO_93
DSS_PCLK/GPIO_66/HW_DBG12
DSS_HSYNC/GPIO_67/HW_DBG13
DSS_VSYNC/GPIO_68
DSS_ACBIAS/GPIO_69
R10
33
MMC1_CLK/MS_CLK/GPIO_120
MMC1_CMD/MS_BS/GPIO_121
MMC1_DAT0/MS_DAT0/GPIO_122
MMC1_DAT1/MS_DAT1/GPIO_123
MMC1_DAT2/MS_DAT2/GPIO_124
MMC1_DAT3/MS_DAT3/GPIO_125
MMC1_DAT4/SIM_IO/GPIO_126
MMC1_DAT5/SIM_CLK/GPIO_127
MMC1_DAT6/SIM_PWRCTRL/GPIO_128
MMC1_DAT7/SIM_RST/GPIO_129
MMC2_CLK/McSPI3_CLK/GPIO_130
MMC2_CMD/McSPI3_SIMO/GPIO_131
MMC2_DAT0/McSPI3_SOMI/GPIO_132
MMC2_DAT1/GPIO_133
MMC2_DAT2/McSPI3_CS1/GPIO_134
MMC2_DAT3/McSPI3_CS0/GPIO_135
MMC2_DAT4/MMC2_DIR_DAT0/MMC3_DAT0/GPIO_136
MMC2_DAT5/MMC2_DIR_DAT1/CAM_GLOBAL_RESET/MMC3_DAT1/GPIO_137/HSUSB3_TLL_STP/MM3_RXDP
MMC2_DAT6/MMC2_DIR_CMD/CAM_SHUTTER/MMC3_DAT2/GPIO_138/HSUSB3_TLL_DIR
MMC2_DAT7/MMC2_CLKIN/MMC3_DAT3/GPIO_139/HSUSB3_TLL_NXT/MM3_RXDM
SDRC_D31
SDRC_D30
SDRC_D29
SDRC_D28
SDRC_D27
SDRC_D26
SDRC_D25
SDRC_D24
SDRC_D23
SDRC_D22
SDRC_D21
SDRC_D20
SDRC_D19
SDRC_D18
SDRC_D17
SDRC_D16
SDRC_D15
SDRC_D14
SDRC_D13
SDRC_D12
SDRC_D11
SDRC_D10
SDRC_D9
SDRC_D8
SDRC_D7
SDRC_D6
SDRC_D5
SDRC_D4
SDRC_D3
SDRC_D2
SDRC_D1
SDRC_D0
GPMC_A10/SYS_nDMAREQ3/GPIO_43
GPMC_A9/SYS_nDMAREQ2/GPIO_42
GPMC_A8/GPIO_41
GPMC_A7/GPIO_40
GPMC_A6/GPIO_39
GPMC_A5/GPIO_38
GPMC_A4/GPIO_37
GPMC_A3/GPIO_36
GPMC_A2/GPIO_35
GPMC_A1/GPIO_34
GPMC_D15/GPIO_51
GPMC_D14/GPIO_50
GPMC_D13/GPIO_49
GPMC_D12/GPIO_48
GPMC_D11/GPIO_47
GPMC_D10/GPIO_46
GPMC_D9/GPIO_45
GPMC_D8/GPIO_44
GPMC_D7
GPMC_D6
GPMC_D5
GPMC_D4
GPMC_D3
GPMC_D2
GPMC_D1
GPMC_D0
GPMC_nCS0
GPMC_nCS1/GPIO_52
GPMC_nCS2/GPIO_53
GPMC_nCS3/SYS_nDMAREQ0/GPIO_54
GPMC_nCS4/SYS_nDMAREQ1/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55
GPMC_nCS5/SYS_nDMAREQ2/McBSP4_DR/GPT10_PWM_EVT/GPIO_56
GPMC_nCS6/SYS_nDMAREQ3/McBSP4_DX/GPT11_PWM_EVT/GPIO_57
GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58
GPMC_CLK/GPIO_59
GPMC_nWE
GPMC_nOE
GPMC_nADV_ALE
GPMC_nBE0_CLE/GPIO_60
GPMC_nBE1/GPIO_61
GPMC_nWP/GPIO_62
GPMC_WAIT0
GPMC_WAIT1/GPIO_63
GPMC_WAIT2/GPIO_64
GPMC_WAIT3/SYS_nDMAREQ1/GPIO_65
UART2_CTS/McBSP3_DX/GPT9_PWMEVT/GPIO_144
UART2_RTS/McBSP3_DR/GPT10_PWMEVT/GPIO_145
UART2_TX/McBSP3_CLKX/GPT11_PWMEVT/GPIO_146
UART2_RX/McBSP3_FSX/GPT8_PWMEVT/GPIO_147
UART3_CTS_RCTX/GPIO_163
UART3_RTS_SD/GPIO_164
UART3_RX_IRRX/GPIO_165
UART3_TX_IRTX/GPIO_166
VIO_1V8
GPMC_WAIT0
R110
1K,0603
MCBSP3_DX 8
MCBSP3_DR 8
MCBSP3_CLKX 8
USB2HS_nRST 9
UART3_RX 9
UART3_TX 9
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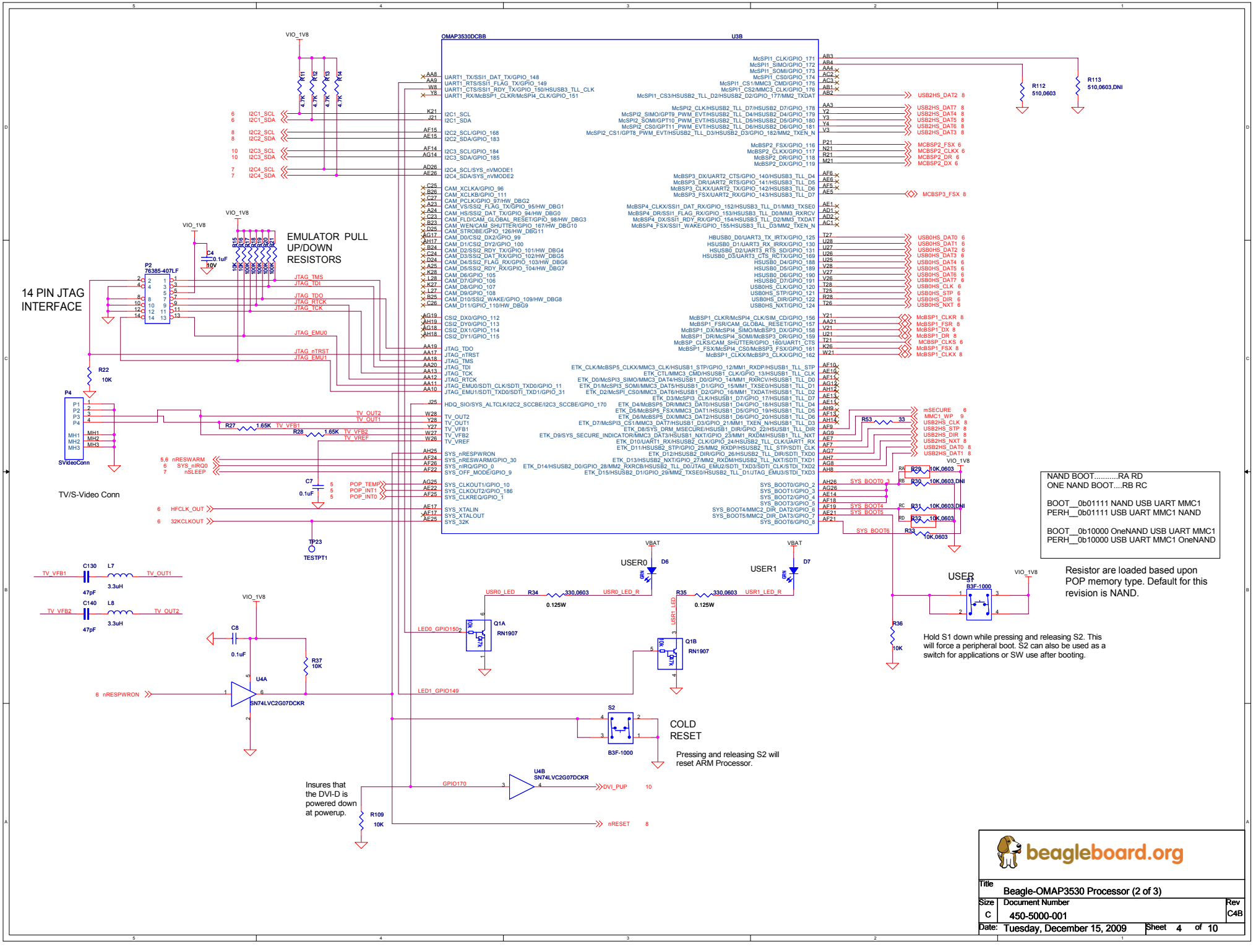

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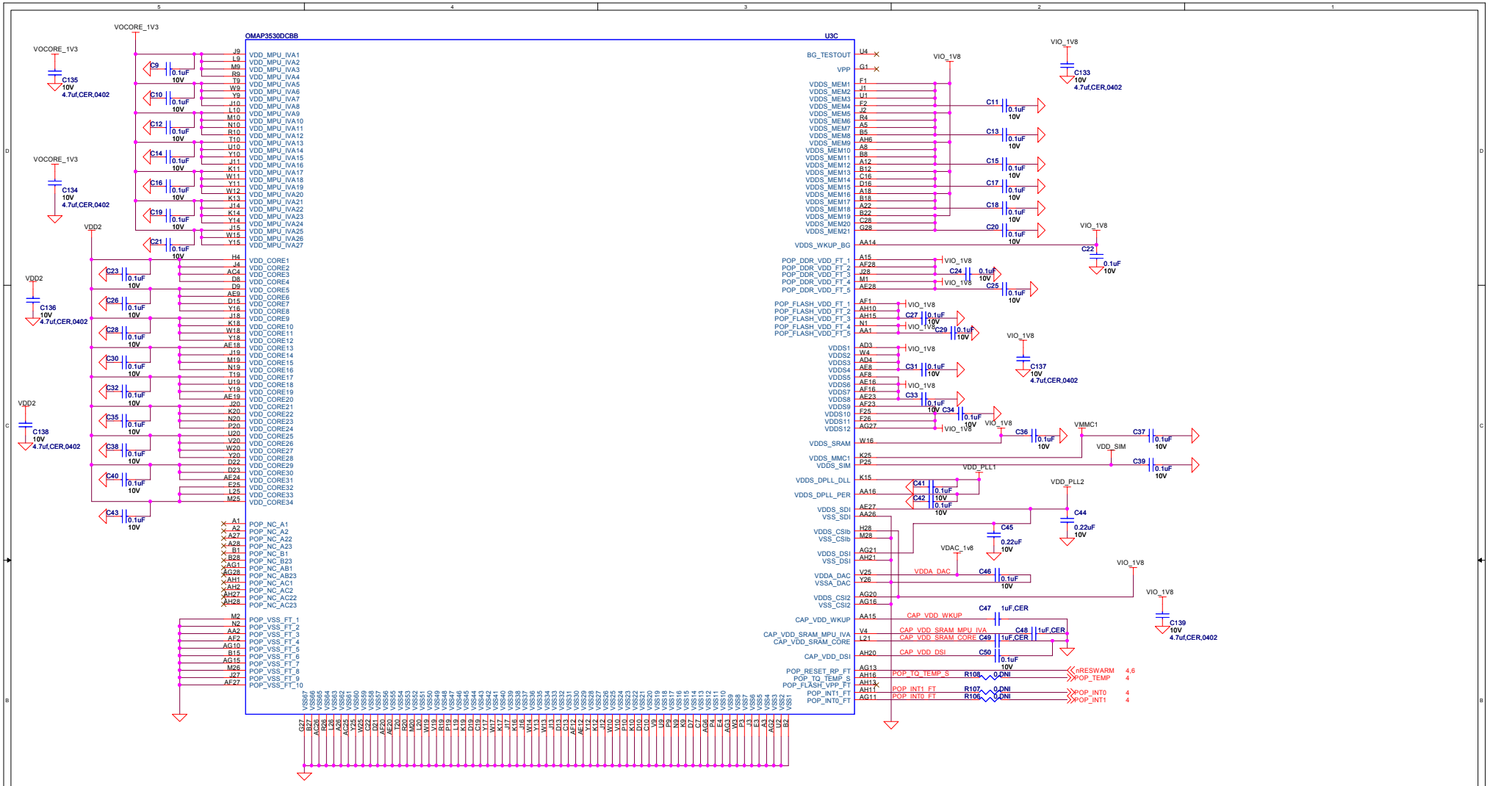
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VDD2
VIO_1V8
VDAC_1v8
VDD_PLL1
VDD_PLL2
VMMC1
VDD_SIM
VDD_CORE1
VDD_CORE2
VDD_CORE3
VDD_CORE4
VDD_CORE5
VDD_CORE6
VDD_CORE7
VDD_CORE8
VDD_CORE9
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VDD_CORE26
VDD_CORE27
VDD_CORE28
VDD_CORE29
VDD_CORE30
VDD_CORE31
VDD_CORE32
VDD_CORE33
VDD_CORE34
VDD_MPU_IVA1
VDD_MPU_IVA2
VDD_MPU_IVA3
VDD_MPU_IVA4
VDD_MPU_IVA5
VDD_MPU_IVA6
VDD_MPU_IVA7
VDD_MPU_IVA8
VDD_MPU_IVA9
VDD_MPU_IVA10
VDD_MPU_IVA11
VDD_MPU_IVA12
VDD_MPU_IVA13
VDD_MPU_IVA14
VDD_MPU_IVA15
VDD_MPU_IVA16
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VDD_MPU_IVA22
VDD_MPU_IVA23
VDD_MPU_IVA24
VDD_MPU_IVA25
VDD_MPU_IVA26
VDD_MPU_IVA27
POP_NC_A1
POP_NC_A2
POP_NC_A22
POP_NC_A23
POP_NC_B1
POP_NC_B23
POP_NC_AB1
POP_NC_AB23
POP_NC_AC1
POP_NC_AC2
POP_NC_AC22
POP_NC_AC23
POP_VSS_FT_1
POP_VSS_FT_2
POP_VSS_FT_3
POP_VSS_FT_4
POP_VSS_FT_5
POP_VSS_FT_6
POP_VSS_FT_7
POP_VSS_FT_8
POP_VSS_FT_9
POP_VSS_FT_10
BG_TESTOUT
VPP
VDDS_MEM1
VDDS_MEM2
VDDS_MEM3
VDDS_MEM4
VDDS_MEM5
VDDS_MEM6
VDDS_MEM7
VDDS_MEM8
VDDS_MEM9
VDDS_MEM10
VDDS_MEM11
VDDS_MEM12
VDDS_MEM13
VDDS_MEM14
VDDS_MEM15
VDDS_MEM16
VDDS_MEM17
VDDS_MEM18
VDDS_MEM19
VDDS_MEM20
VDDS_MEM21
VDDS_WKUP_BG
POP_DDR_VDD_FT_1
POP_DDR_VDD_FT_2
POP_DDR_VDD_FT_3
POP_DDR_VDD_FT_4
POP_DDR_VDD_FT_5
POP_FLASH_VDD_FT_1
POP_FLASH_VDD_FT_2
POP_FLASH_VDD_FT_3
POP_FLASH_VDD_FT_4
POP_FLASH_VDD_FT_5
VDDS1
VDDS2
VDDS3
VDDS4
VDDS5
VDDS6
VDDS7
VDDS8
VDDS9
VDDS10
VDDS11
VDDS12
VDDS_SRAM
VDDS_MMC1
VDDS_SIM
VDDS_DPLL_DLL
VDDS_DPLL_PER
VDDS_SDI
VSS_SDI
VDDS_CSIb
VSS_CSIb
VDDS_DSI
VSS_DSI
VDDA_DAC
VSSA_DAC
VDDS_CSI2
VSS_CSI2
CAP_VDD_WKUP
CAP_VDD_SRAM_MPU_IVA
CAP_VDD_SRAM_CORE
CAP_VDD_DSI
POP_RESET_RP_FT
POP_TO_TEMP_S
POP_FLASH_VPP_FT
POP_INT1_FT
POP_INT0_FT
CAP_VDD_WKUP
CAP_VDD_SRAM_MPU_IVA
CAP_VDD_SRAM_CORE
CAP_VDD_DSI
VDDA_DAC
POP_TO_TEMP_S
POP_INT1_FT
POP_INT0_FT
nRESWARM
POP_TEMP
POP_INT0
POP_INT1
R108 0 DNI
R107 0 DNI
R106 0 DNI
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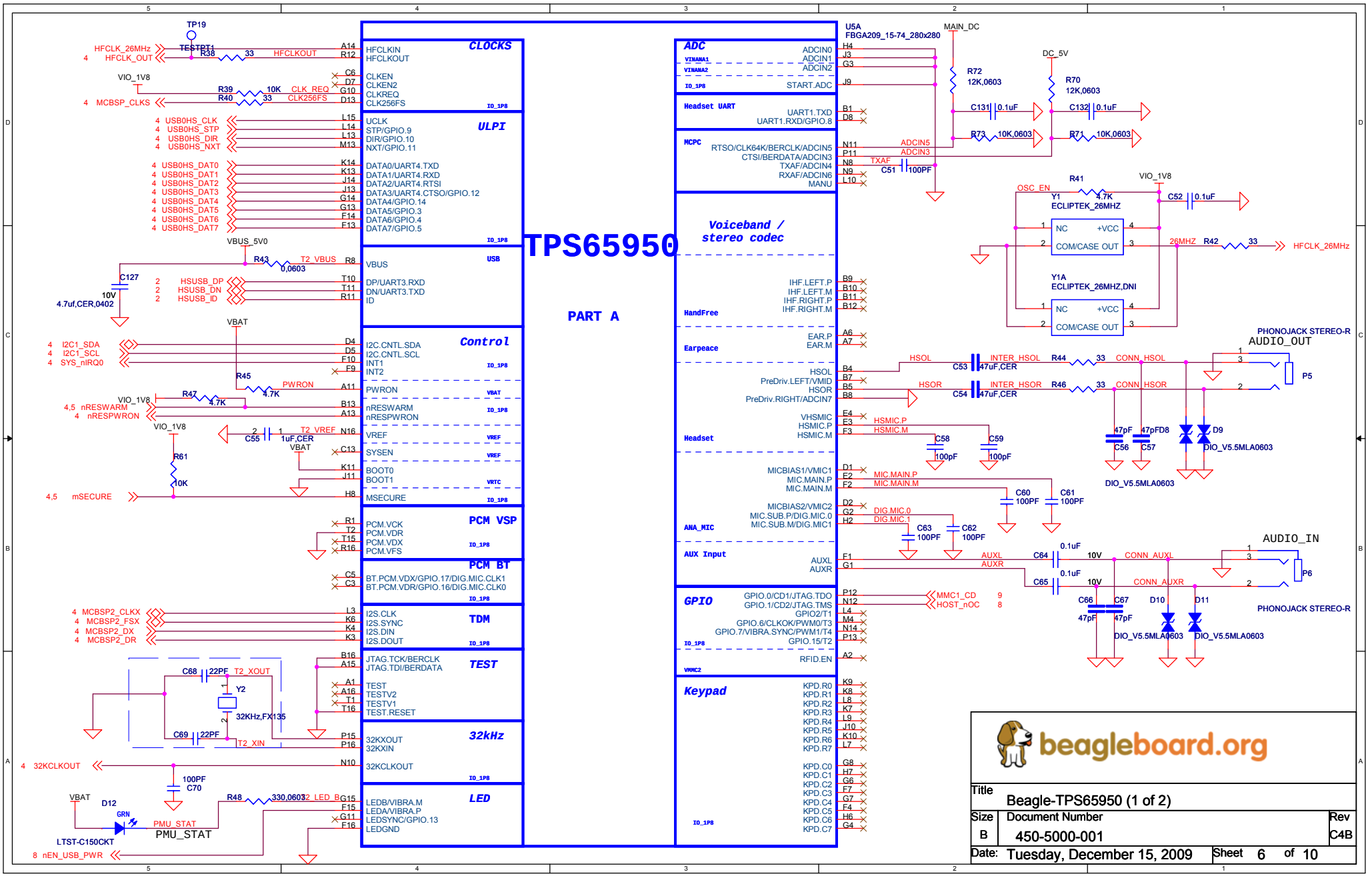

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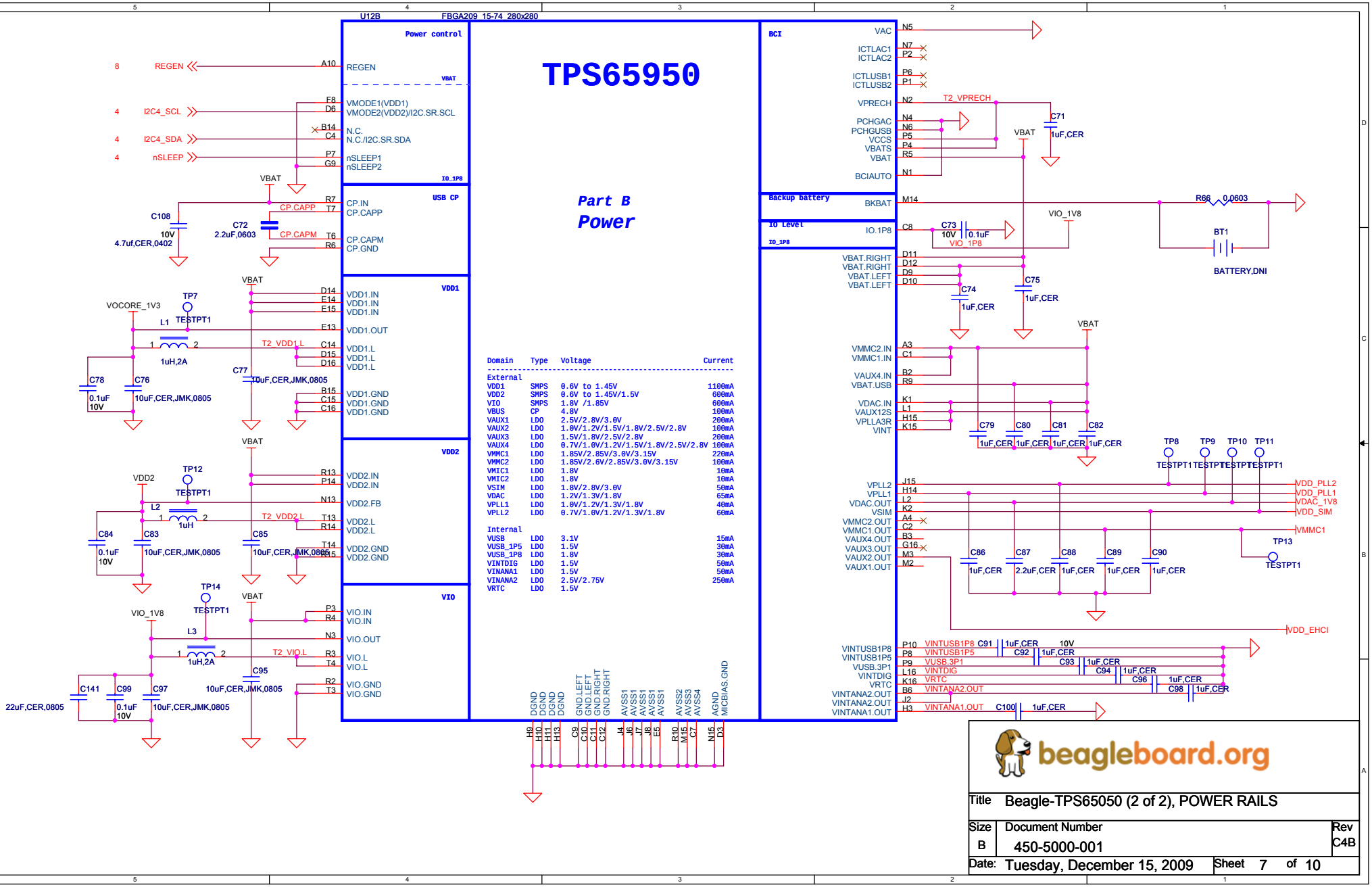

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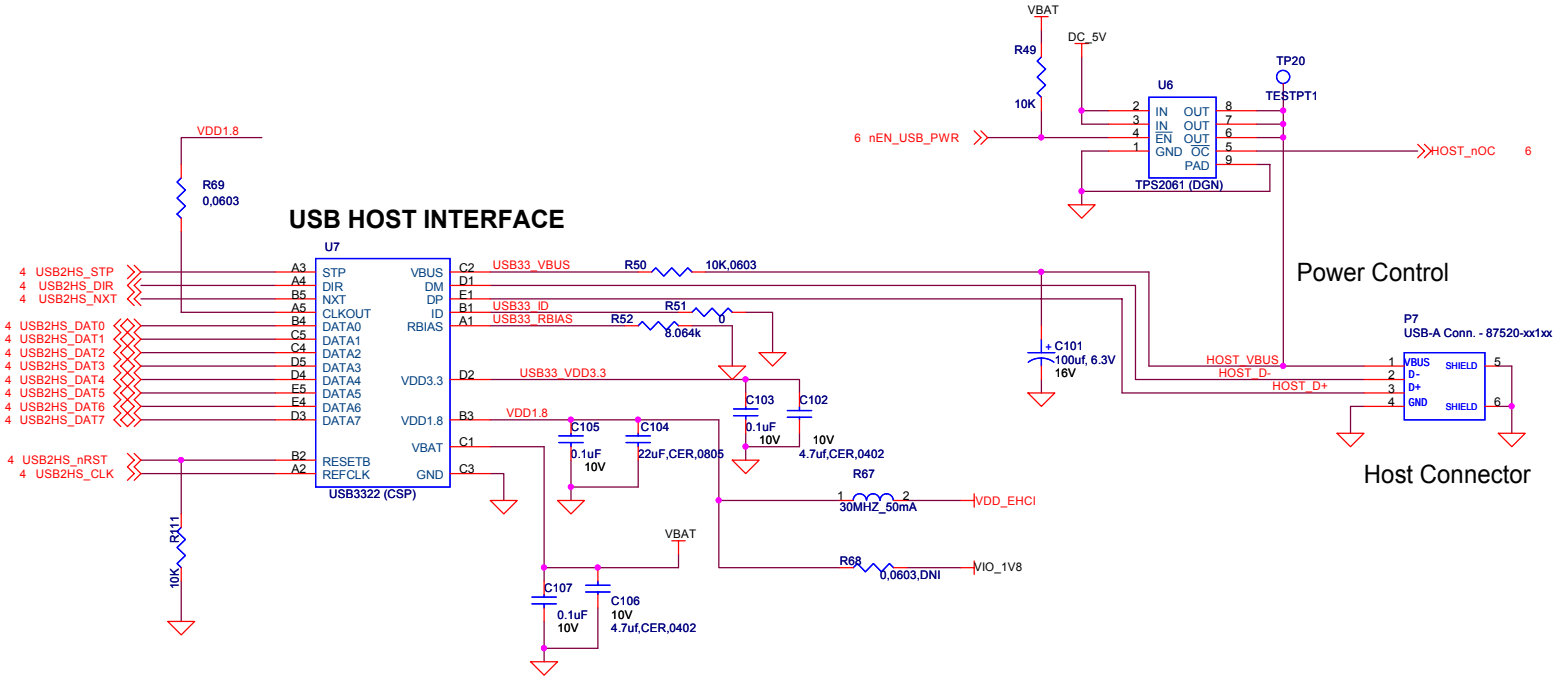

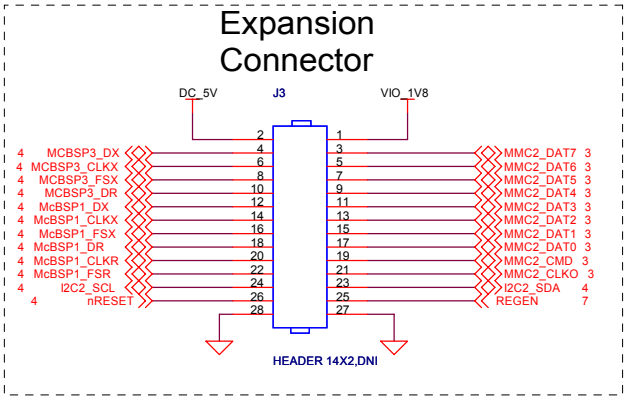

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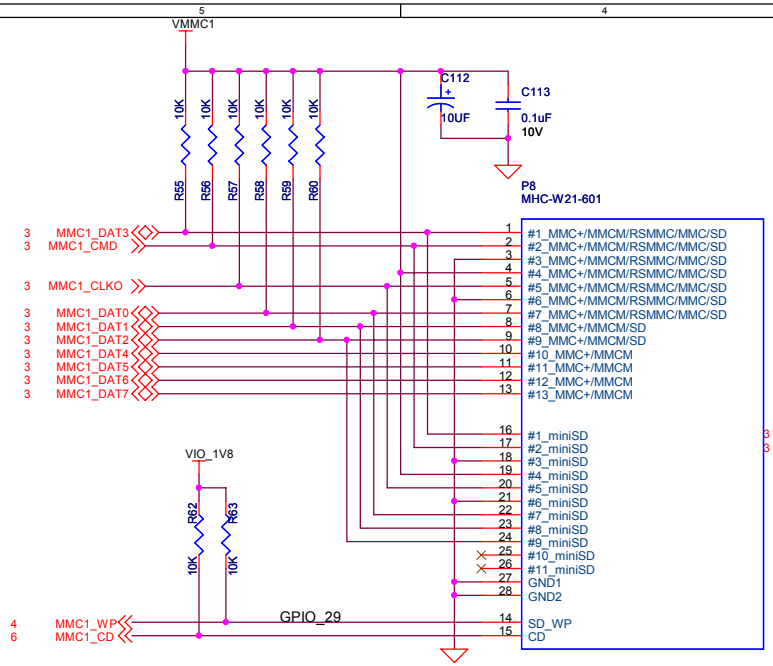
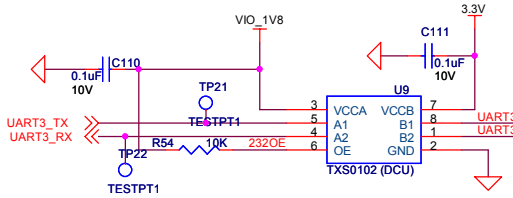
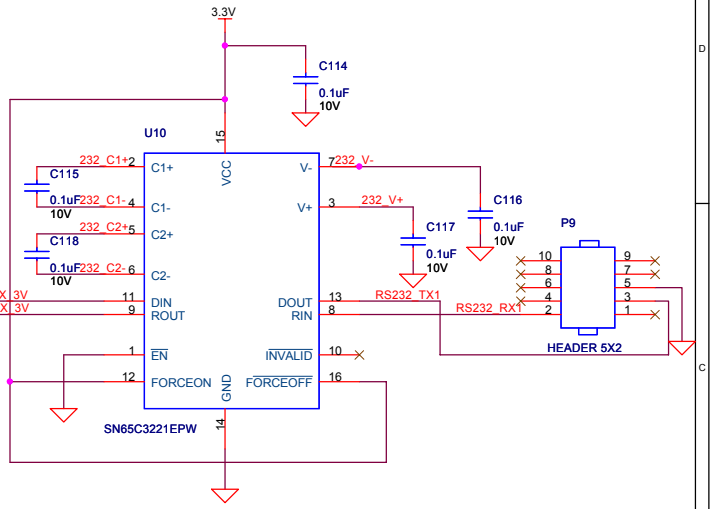
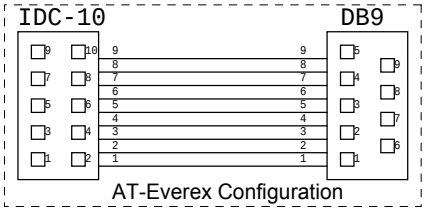


SD/MMC Connector 6 in 1
MMC+, MMCMobile, SD,
MMC, miniSD, RS-MMC



UART3 Serial Port





AT-Everex Configuration

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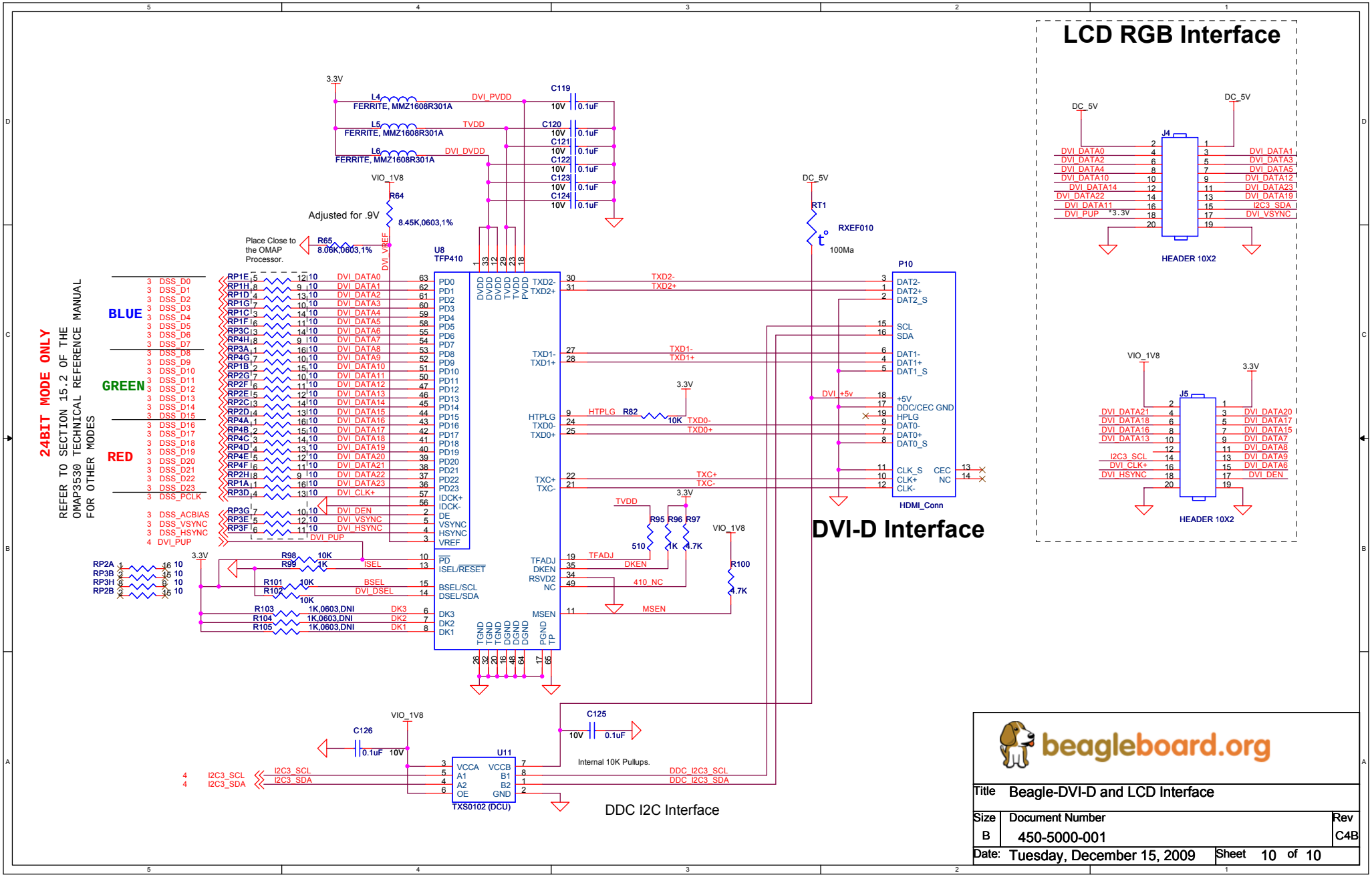
24BIT MODE ONLY
REFER TO SECTION 15.2 OF THE
OMAP3530 TECHNICAL REFERENCE MANUAL
FOR OTHER MODES
BLUE
GREEN
RED
DVI-D Interface
DDC I2C Interface
U8
TFP410
U11
TXS0102 (DCU)
HDMI_Conn
P10
RT1
RXEF010
100Ma
Adjusted for .9V
8.45K,0603,1%
Place Close to the OMAP Processor.
R65
8.06K,0603,1%
Internal 10K Pullups.
LCD RGB Interface
J4
J5
HEADER 10X2
HEADER 10X2
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