


REV	DESCRIPTION	DATE	BY
A	<p>FEATURE CHANGES</p> <ol style="list-style-type: none"> Added 4 port LS/FS/HS HUB to provide four USB Host ports. Made connection for the 1.8V rail on the USB PHY to go to VAUX2. Added camera connector that is compatible to the Leopard Imaging Camera modules. Added power management capabilities to allow shut down of serial port, DVI-D, and power LED. Switched to DM3730 processor and 512MB memory. Added ability to turn off 26MHZ oscillator. Increased overall board size to accomodate the changes. Changed serial connector to a female DB9. Added a 10/100 Ethernet port. 	8/31/09	GC
A1	<ol style="list-style-type: none"> Disabled the DVI-D powerdown due to use of wrong GPIO pin. Pin is in the MMC group and it cannot be switched to 1.8V without impacting the SD card slot. Disables HUB reset due to a timing issue with SW. When active the LAN9514 would not work correctly and the Ethernet function is broken. 	5/13/10	GC
A2	<ol style="list-style-type: none"> Changed C9 to DNI and changed R34, 4.7K to installed to enable the S-Video operation. 	6/15/10	GC
A3	<p>NO MAJOR FEATURE CHANGES.</p> <ol style="list-style-type: none"> PCB Layout changes. Added R157 in series with MMC2_CLK. Added R158 to isolate shunt FET to reduce power in DC mode. Added optional pullup resistors on I2C2_SCL and I2C_SDA into the layout. Moved DVI_PUP signal to TPS65950. Previous location could not be used due to a conflict with the MMC function on the pins. 	6/23/10	GC

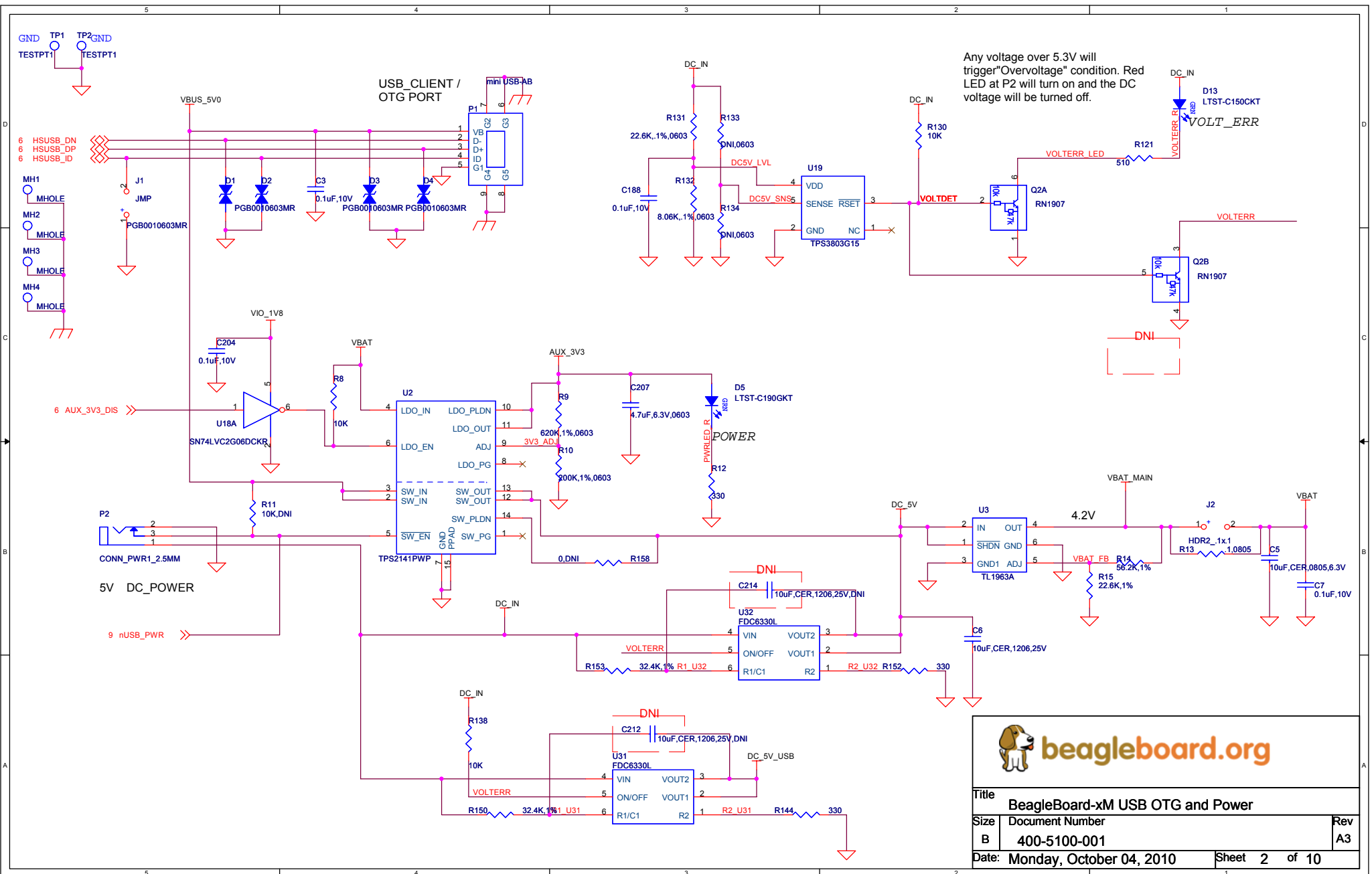
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7	PMIC, POWER RAILS
8	MICROSD, RS232,CAMERA,EXPANSION
9	DVI-D, LCD EXPANSION
10	USB HOST, HUB, ETHERNET

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Any voltage over 5.3V will trigger "Overvoltage" condition. Red LED at P2 will turn on and the DC voltage will be turned off.



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- × H10 SDCR_BA1
- × H9 SDCR_BA0
- × E1 SDCR_A14
- × E2 SDCR_A13
- × D1 SDCR_A12
- × D3 SDCR_A11
- × D4 SDCR_A10
- × A9 SDCR_A9
- × C1 SDCR_A8
- × C2 SDCR_A7
- × C3 SDCR_A6
- × D5 SDCR_A5
- × C4 SDCR_A4
- × C5 SDCR_A3
- × B3 SDCR_A2
- × B4 SDCR_A1
- × A4 SDCR_A0

- × H14 SDCR_nRAS
- × H13 SDCR_nCAS
- × H15 SDCR_nWE
- × A13 SDCR_CLK
- × A14 SDCR_nCLK
- × H16 SDCR_CKE1
- × H12 SDCR_CKE0
- × H11 SDCR_nCS1
- × C20 SDCR_nCS0
- × B11 SDCR_DM3
- × A16 SDCR_DM2
- × E7 SDCR_DM1
- × A20 SDCR_DM0
- × A10 SDCR_DQS3
- × A17 SDCR_DQS2
- × A6 SDCR_DQS1

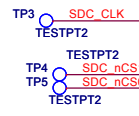
- AG22 DSS_D0/DX0/UART1_CTS/DSSVENC656_DATA0/GPIO_70
- AH22 DSS_D1/DY0/UART1_RTS/DSSVENC656_DATA1/GPIO_71
- AG23 DSS_D2/DX1/DSSVENC656_DATA2/GPIO_72
- AH23 DSS_D3/DY1/DSSVENC656_DATA3/GPIO_73
- AG24 DSS_D4/DX2/UART3_RX_IRRX/DSSVENC656_DATA4/GPIO_74
- AH24 DSS_D5/DY2/UART3_TX_IRTX/DSSVENC656_DATA5/GPIO_75
- E26 DSS_D6/UART1_TX/DSSVENC656_DATA6/GPIO_76/HW_DBG14
- F28 DSS_D7/UART1_RX/DSSVENC656_DATA7/GPIO_77/HW_DBG15
- E27 DSS_D8/GPIO_78/HW_DBG16
- G26 DSS_D9/GPIO_79/HW_DBG17
- AD28 DSS_D10/SDI_DAT1N/GPIO_80
- AD27 DSS_D11/SDI_DAT1P/GPIO_81
- AB28 DSS_D12/SDI_DAT2N/GPIO_82
- AB27 DSS_D13/SDI_DAT2P/GPIO_83
- AA27 DSS_D14/SDI_DAT3N/GPIO_84
- AA27 DSS_D15/SDI_DAT3P/GPIO_85
- G25 DSS_D16/GPIO_86
- H27 DSS_D17/GPIO_87
- H26 DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88
- H25 DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89
- E28 DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_D2/GPIO_90
- J26 DSS_D21/SDI_STP/McSPI3_CS0/DSS_D3/GPIO_91
- AC27 DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92
- AC28 DSS_D23/SDI_CLKN/DSS_D5/GPIO_93
- D28 DSS_PCLK/GPIO_66/HW_DBG12
- D26 DSS_HSYNC/GPIO_67/HW_DBG13
- D27 DSS_VSYNC/GPIO_68
- E27 DSS_ACBIAS/GPIO_69

- × R16 MMC1_CLK0
- × M27 MMC1_CMD
- × N27 MMC1_DAT0
- × N26 MMC1_DAT1
- × N25 MMC1_DAT2
- × P28 MMC1_DAT3
- × P27 MMC1_DAT4
- × P26 MMC1_DAT5
- × R27 MMC1_DAT6
- × R25 MMC1_DAT7

- × AE2 MMC2_CLK0
- × AG5 MMC2_CMD
- × AH5 MMC2_DAT0
- × AH4 MMC2_DAT1
- × AC4 MMC2_DAT2
- × AF4 MMC2_DAT3
- × AF4 MMC2_DAT4
- × AH3 MMC2_DAT5
- × AF3 MMC2_DAT6
- × AE3 MMC2_DAT7

- × AE2 MMC2_CLK/McSPI3_CLK/GPIO_130
- × AG5 MMC2_CMD/McSPI3_SIMO/GPIO_131
- × AH5 MMC2_DAT0/McSPI3_SOMI/GPIO_132
- × AH4 MMC2_DAT1/GPIO_133
- × AC4 MMC2_DAT2/McSPI3_CS1/GPIO_134
- × AF4 MMC2_DAT3/McSPI3_CS0/GPIO_135
- × AF4 MMC2_DAT4/McSPI3_CS0/GPIO_136
- × AH3 MMC2_DAT5/McSPI3_CS0/GPIO_137
- × AF3 MMC2_DAT6/McSPI3_CS0/GPIO_138
- × AE3 MMC2_DAT7/McSPI3_CS0/GPIO_139

- DSS_D0/DX0/UART1_CTS/DSSVENC656_DATA0/GPIO_70
- DSS_D1/DY0/UART1_RTS/DSSVENC656_DATA1/GPIO_71
- DSS_D2/DX1/DSSVENC656_DATA2/GPIO_72
- DSS_D3/DY1/DSSVENC656_DATA3/GPIO_73
- DSS_D4/DX2/UART3_RX_IRRX/DSSVENC656_DATA4/GPIO_74
- DSS_D5/DY2/UART3_TX_IRTX/DSSVENC656_DATA5/GPIO_75
- DSS_D6/UART1_TX/DSSVENC656_DATA6/GPIO_76/HW_DBG14
- DSS_D7/UART1_RX/DSSVENC656_DATA7/GPIO_77/HW_DBG15
- DSS_D8/GPIO_78/HW_DBG16
- DSS_D9/GPIO_79/HW_DBG17
- DSS_D10/SDI_DAT1N/GPIO_80
- DSS_D11/SDI_DAT1P/GPIO_81
- DSS_D12/SDI_DAT2N/GPIO_82
- DSS_D13/SDI_DAT2P/GPIO_83
- DSS_D14/SDI_DAT3N/GPIO_84
- DSS_D15/SDI_DAT3P/GPIO_85
- DSS_D16/GPIO_86
- DSS_D17/GPIO_87
- DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88
- DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89
- DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_D2/GPIO_90
- DSS_D21/SDI_STP/McSPI3_CS0/DSS_D3/GPIO_91
- DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92
- DSS_D23/SDI_CLKN/DSS_D5/GPIO_93
- DSS_PCLK/GPIO_66/HW_DBG12
- DSS_HSYNC/GPIO_67/HW_DBG13
- DSS_VSYNC/GPIO_68
- DSS_ACBIAS/GPIO_69
- MMC1_CLK/MS_CLK/GPIO_120
- MMC1_CMD/MS_BS/GPIO_121
- MMC1_DAT0/MS_DAT0/GPIO_122
- MMC1_DAT1/MS_DAT1/GPIO_123
- MMC1_DAT2/MS_DAT2/GPIO_124
- MMC1_DAT3/MS_DAT3/GPIO_125
- MMC1_DAT4/SIM_IO/GPIO_126
- MMC1_DAT5/SIM_CLK/GPIO_127
- MMC1_DAT6/SIM_PWRCTRL/GPIO_128
- MMC1_DAT7/SIM_RST/GPIO_129
- MMC2_CLK/McSPI3_CLK/GPIO_130
- MMC2_CMD/McSPI3_SIMO/GPIO_131
- MMC2_DAT0/McSPI3_SOMI/GPIO_132
- MMC2_DAT1/GPIO_133
- MMC2_DAT2/McSPI3_CS1/GPIO_134
- MMC2_DAT3/McSPI3_CS0/GPIO_135
- MMC2_DAT4/McSPI3_CS0/GPIO_136
- MMC2_DAT5/McSPI3_CS0/GPIO_137
- MMC2_DAT6/McSPI3_CS0/GPIO_138
- MMC2_DAT7/McSPI3_CS0/GPIO_139



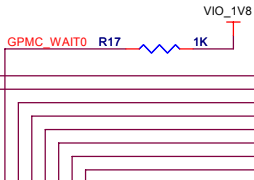
- SDRC_D31 B21
- SDRC_D30 A21
- SDRC_D29 D20
- SDRC_D28 B20
- SDRC_D27 B19
- SDRC_D26 A19
- SDRC_D25 C18
- SDRC_D24 D14
- SDRC_D23 B13
- SDRC_D22 A11
- SDRC_D21 C12
- SDRC_D20 D12
- SDRC_D19 C11
- SDRC_D18 B10
- SDRC_D17 D11
- SDRC_D16 B18
- SDRC_D15 A17
- SDRC_D14 D17
- SDRC_D13 B16
- SDRC_D12 C15
- SDRC_D11 B14
- SDRC_D10 C14
- SDRC_D9 A9
- SDRC_D8 B9
- SDRC_D7 A7
- SDRC_D6 C9
- SDRC_D5 C8
- SDRC_D4 B6
- SDRC_D3 C6
- SDRC_D2 D6
- SDRC_D1 K3
- SDRC_D0 L3

- GPMC_A10/SYS_nDMAREQ3/GPIO_43 M3
- GPMC_A9/SYS_nDMAREQ2/GPIO_42 N3
- GPMC_A8/GPIO_41 R3
- GPMC_A7/GPIO_40 T3
- GPMC_A6/GPIO_39 K4
- GPMC_A5/GPIO_38 L4
- GPMC_A4/GPIO_37 M4
- GPMC_A3/GPIO_36 N4
- GPMC_A2/GPIO_35 Y1
- GPMC_A1/GPIO_34 W1

- GPMC_D15/GPIO_51 T2
- GPMC_D14/GPIO_50 R2
- GPMC_D13/GPIO_49 R1
- GPMC_D12/GPIO_48 P1
- GPMC_D11/GPIO_47 K2
- GPMC_D10/GPIO_46 H2
- GPMC_D9/GPIO_45 W2
- GPMC_D8/GPIO_44 V2
- GPMC_D7 GPMc_D6
- GPMC_D6 GPMc_D5
- GPMC_D5 GPMc_D4
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- GPMC_D3 GPMc_D2
- GPMC_D2 GPMc_D1
- GPMC_D1 GPMc_D0

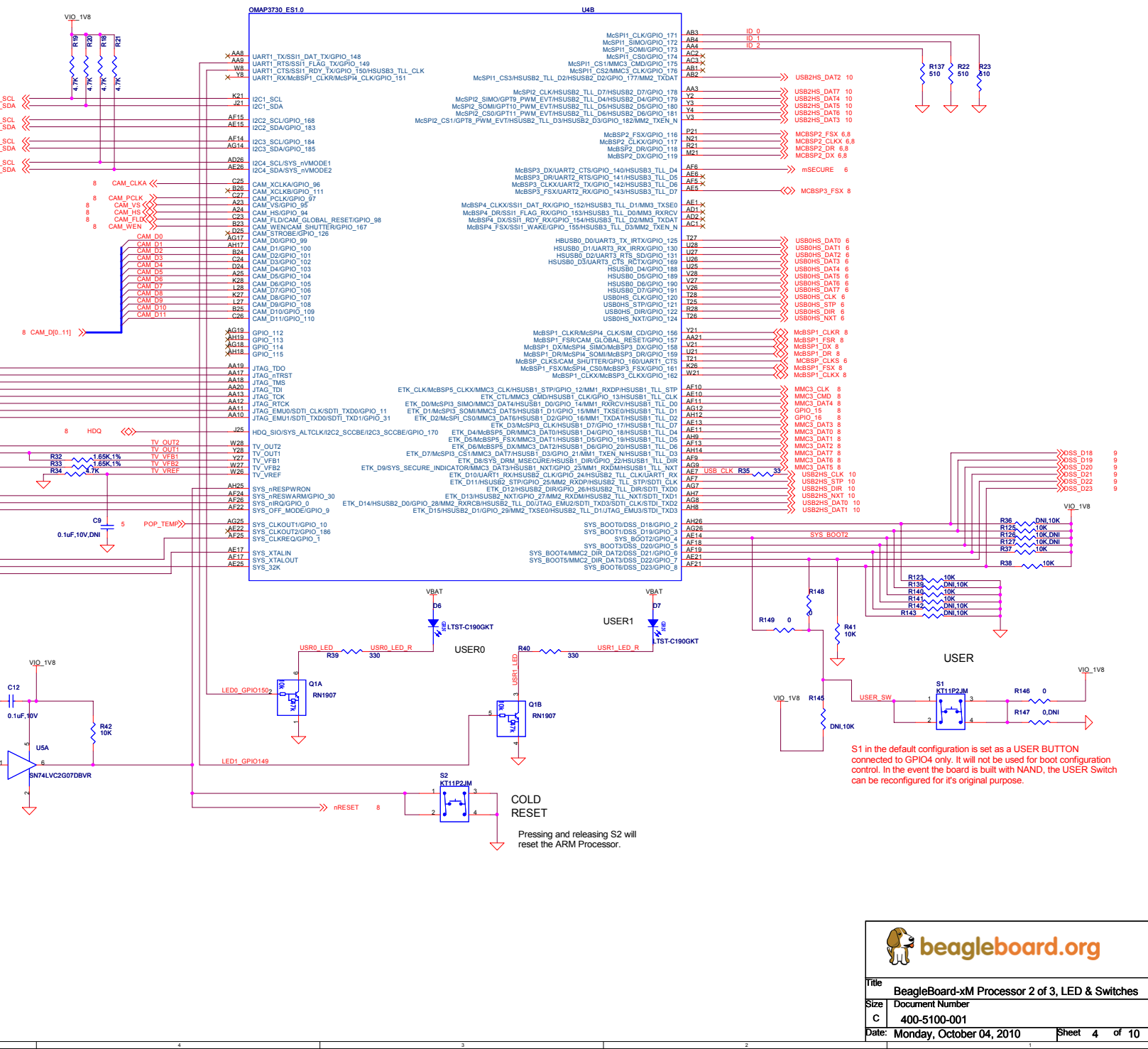
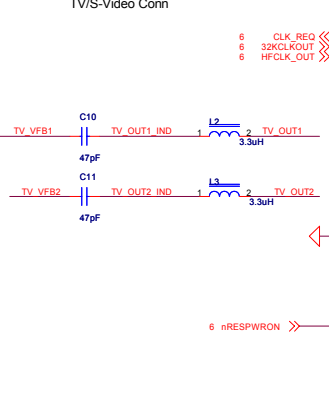
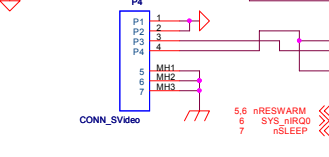
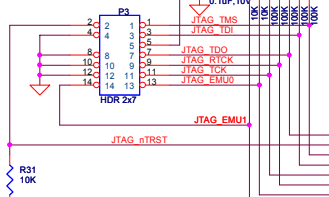
- GPMC_nCS0 G4
- GPMC_nCS1/GPIO_52 H3
- GPMC_nCS2/GPIO_53 V8
- GPMC_nCS3/GPIO_54 U8
- GPMC_nCS4/SYS_nDMAREQ1/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55 T8
- GPMC_nCS5/SYS_nDMAREQ2/McBSP4_DR/GPT11_PWM_EVT/GPIO_56 R8
- GPMC_nCS6/SYS_nDMAREQ3/McBSP4_DX/GPT11_PWM_EVT/GPIO_57 P8
- GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58 N8
- GPMC_CLK/GPIO_59 T4
- GPMC_nWE F4
- GPMC_nOE G2
- GPMC_nADV_ALE F3
- GPMC_nBE0_CLE/GPIO_60 G3
- GPMC_nBE1/GPIO_61 U3
- GPMC_nWP/GPIO_62 H1
- GPMC_WAIT0 M8
- GPMC_WAIT1 L8
- GPMC_WAIT2 K8
- GPMC_WAIT3 J8

- UART2_CTS/McBSP3_DX/GPT9_PWM_EVT/GPIO_144 AB26
- UART2_RTS/McBSP3_DR/GPT10_PWM_EVT/GPIO_145 AB25
- UART2_TX/McBSP3_CLKX/GPT11_PWM_EVT/GPIO_146 AA25
- UART2_RX/McBSP3_FSX/GPT8_PWM_EVT/GPIO_147 AD25
- UART3_CTS_RCTX/GPIO_163 H18
- UART3_RTS_SD/GPIO_164 H18
- UART3_RX_IRRX/GPIO_165 H20
- UART3_TX_IRTX/GPIO_166 H21



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BeagleBoard-xM Processor 1 of 3		
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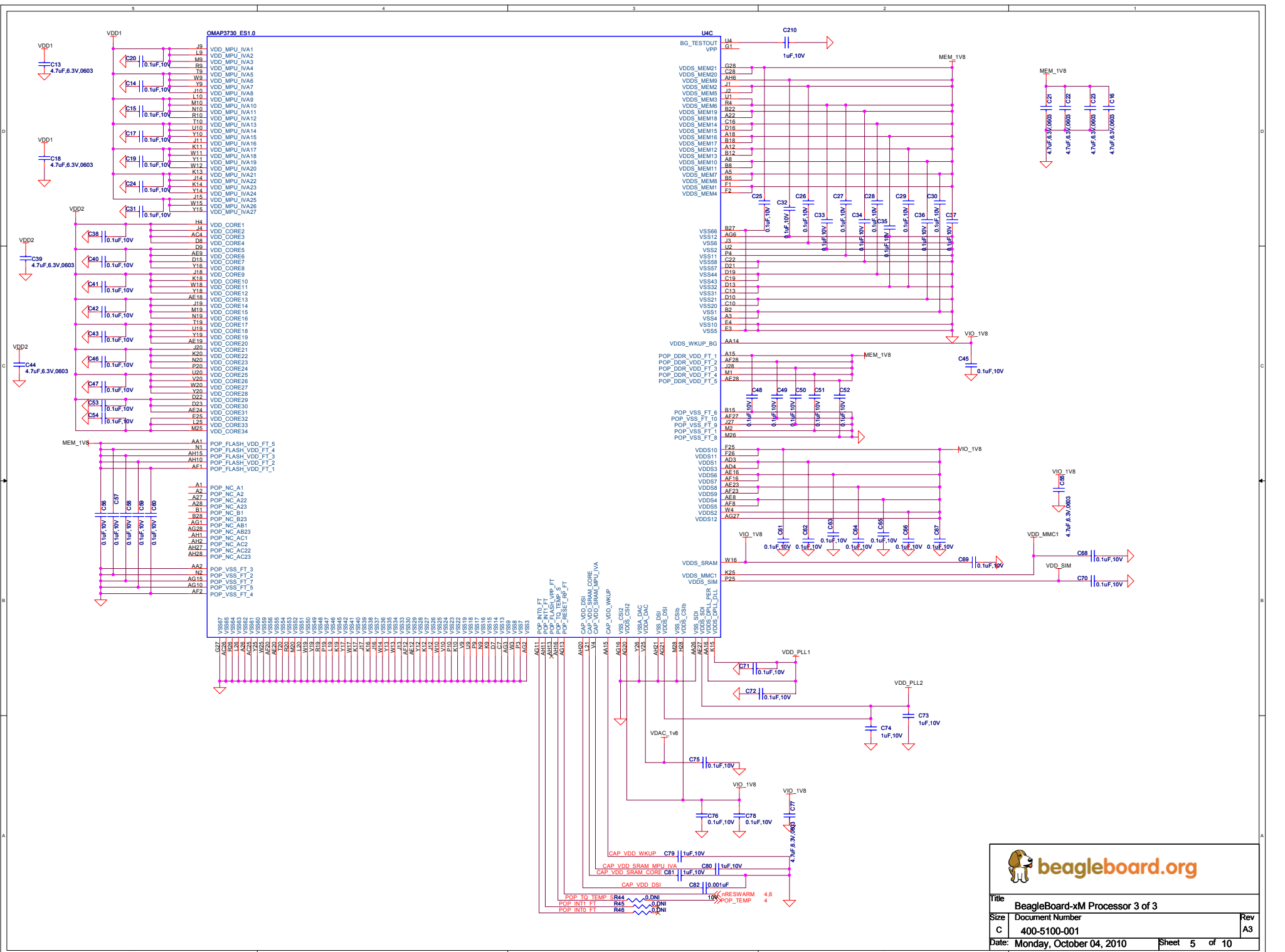
14 PIN JTAG INTERFACE



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BeagleBoard-xM Processor 2 of 3, LED & Switches		
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S1 in the default configuration is set as a USER BUTTON connected to GPIO4 only. It will not be used for boot configuration control. In the event the board is built with NAND, the USER Switch can be reconfigured for it's original purpose.

COLD RESET
Pressing and releasing S2 will reset the ARM Processor.



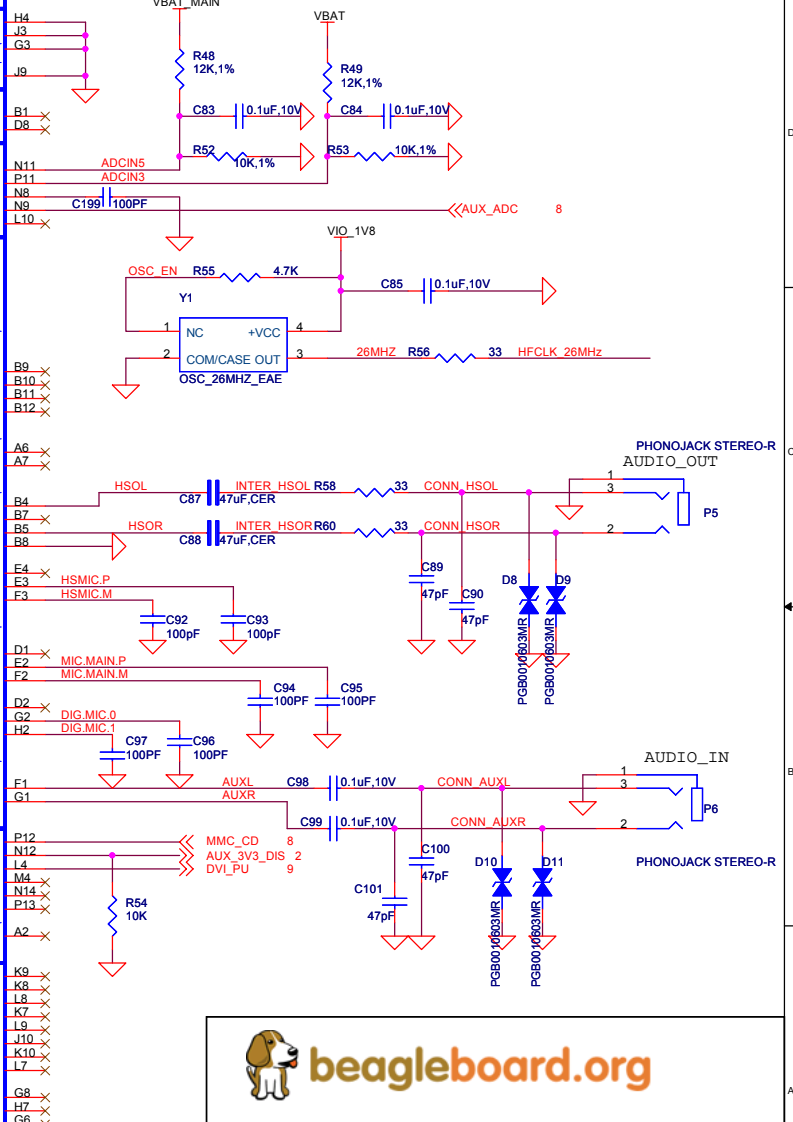
Title BeagleBoard-xM Processor 3 of 3		
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TPS65950

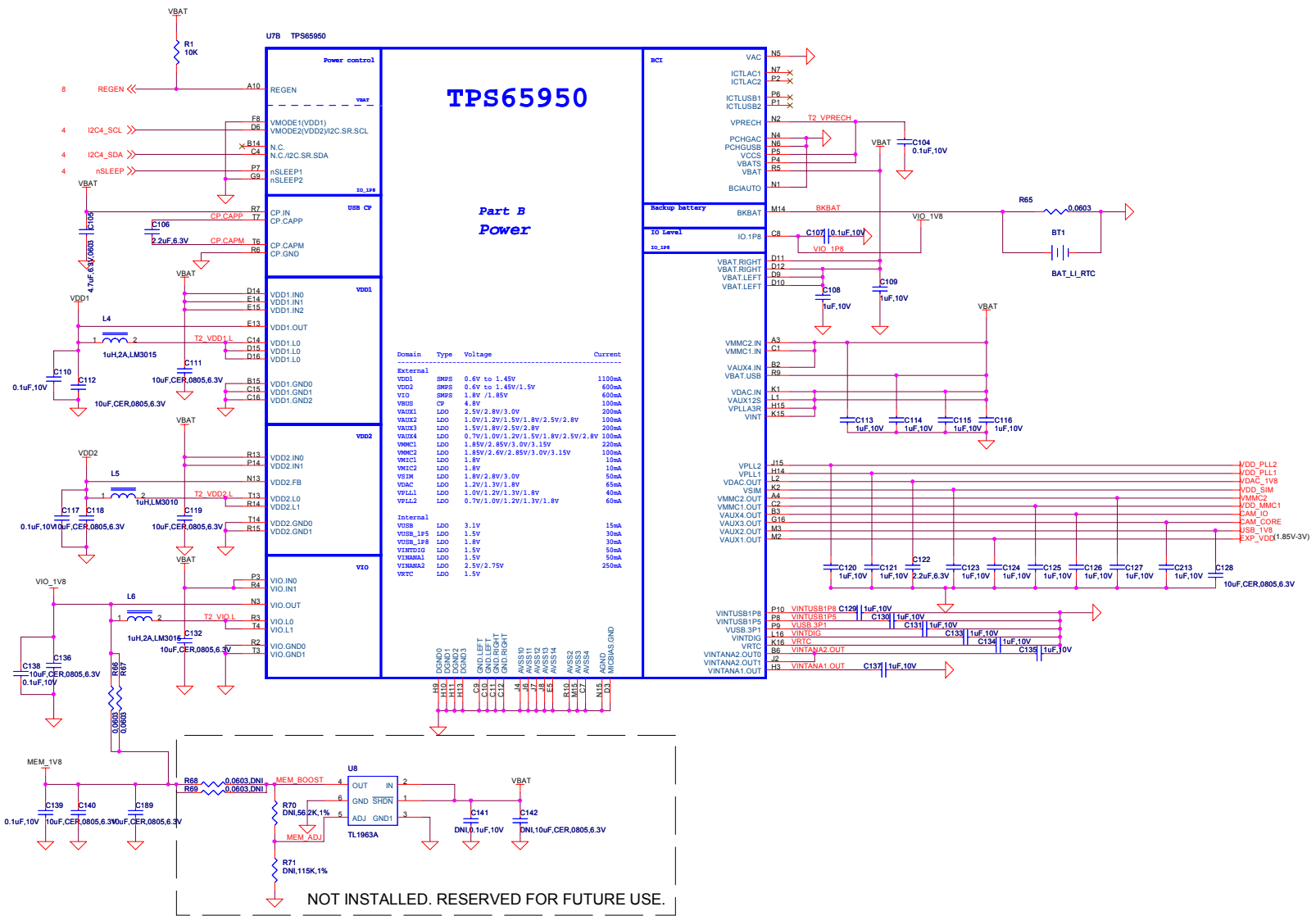
PART A

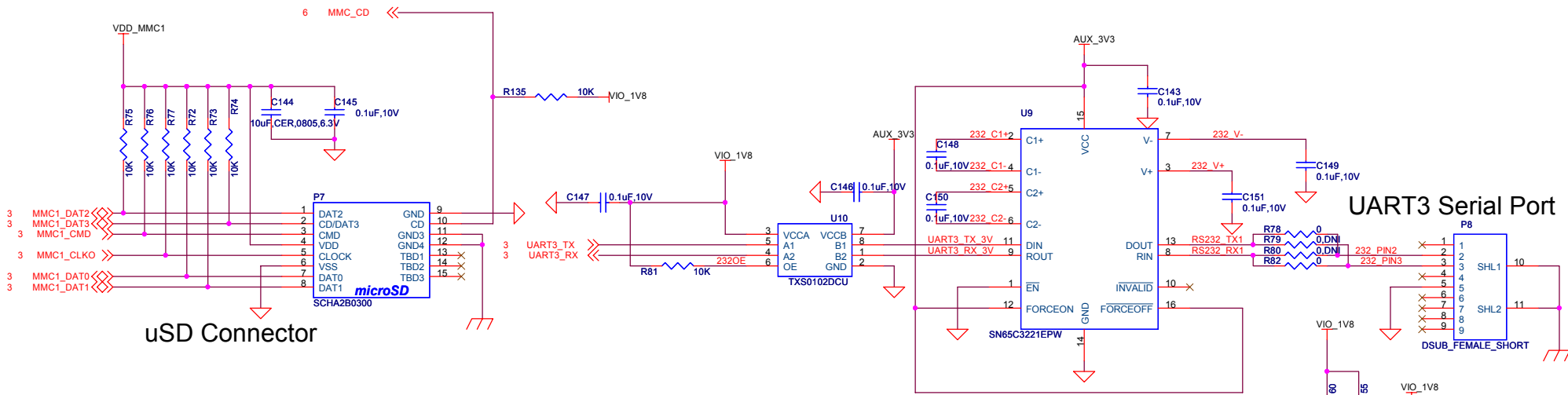
CLOCKS	HFCLKIN HFCLKOUT
ULPI	UCLK STP/GPIO.9 DIR/GPIO.10 NXT/GPIO.11
Control	I2C.CNTL.SDA I2C.CNTL.SCL INT1 INT2
PCM VSP	PCM.VCK PCM.VDR PCM.VDX PCM.VFS
PCM BT	BT.PCM.VDX/GPIO.17/DIG.MIC.CLK1 BT.PCM.VDR/GPIO.16/DIG.MIC.CLK0
TDM	I2S.CLK I2S.SYNC I2S.DIN I2S.DOUT
TEST	JTAG.TCK/BERCLK JTAG.TDI/BERDATA
32kHz	TEST TESTV2 TESTV1 TEST.RESET
LED	LEDB/VIBRA.M LEDA/VIBRA.P LEDSYNC/GPIO.13 LEDGND

ADC	ADCIN0 ADCIN1 ADCIN2 START.ADC
Headset UART	UART1.TXD UART1.RXD/GPIO.8
MCPC	RTSO/CLK64K/BERCLK/ADCIN5 CTS1/BERDATA/ADCIN3 TXAF/ADCIN4 RXAF/ADCIN6 MANU
Voiceband / stereo codec	IHF.LEFT.P IHF.LEFT.M IHF.RIGHT.P IHF.RIGHT.M
HandFree	
Earpiece	EAR.P EAR.M
Headset	VHSMC HSMC.P HSMC.M
ANA_MIC	MICBIAS1/VMIC1 MIC.MAIN.P MIC.MAIN.M
AUX Input	AUXL AUXR
GPIO	GPIO.0/CD1/JTAG.TDO GPIO.1/CD2/JTAG.TMS GPIO2/T1 GPIO.6/CLKOK/PWM0/T3 GPIO.7/VIBRA.SYNC/PWM1/T4 GPIO.15/T2 RFID.EN
Keypad	KPD.R0 KPD.R1 KPD.R2 KPD.R3 KPD.R4 KPD.R5 KPD.R6 KPD.R7 KPD.C0 KPD.C1 KPD.C2 KPD.C3 KPD.C4 KPD.C5 KPD.C6 KPD.C7



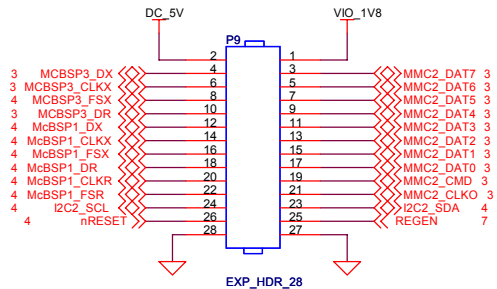
Title BeagleBoard-xM PMIC, AUDIO JACKS, CLOCKS		
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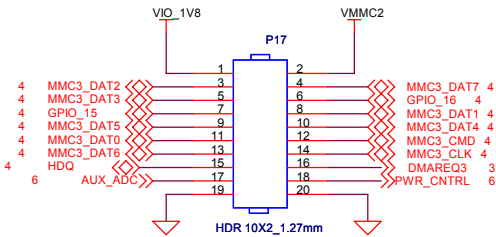


uSD Connector

UART3 Serial Port

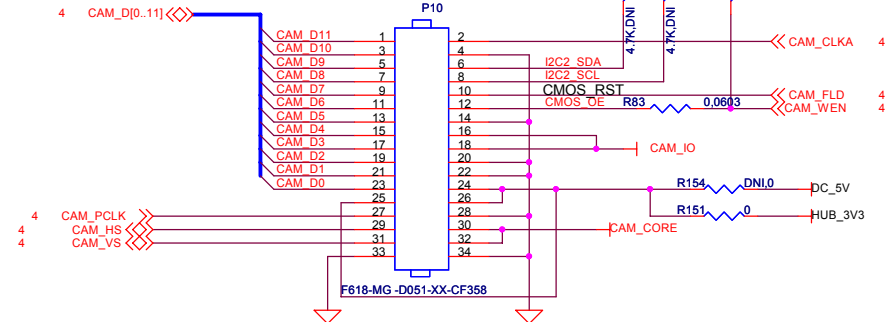
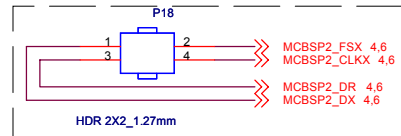


Expansion Connector



AUX ACCESS HEADER

AUDIO ACCESS HEADER



Camera Connector



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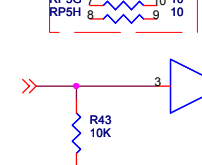
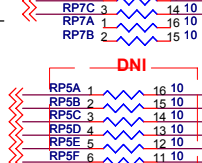
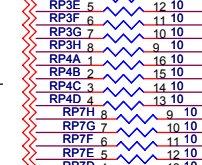
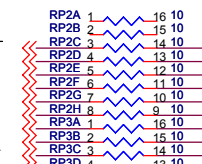
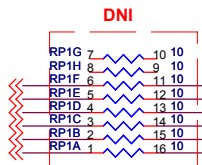
24BIT MODE ONLY
 REFER TO THE PROCESSOR
 TECHNICAL REFERENCE MANUAL
 FOR OTHER MODES

3 DSS_DX0
 3 DSS_DX1
 3 DSS_DX2
 3 DSS_DX3
 3 DSS_DX4
 3 DSS_DX5

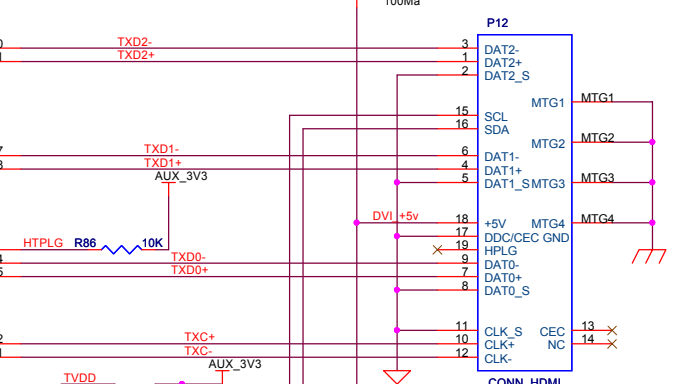
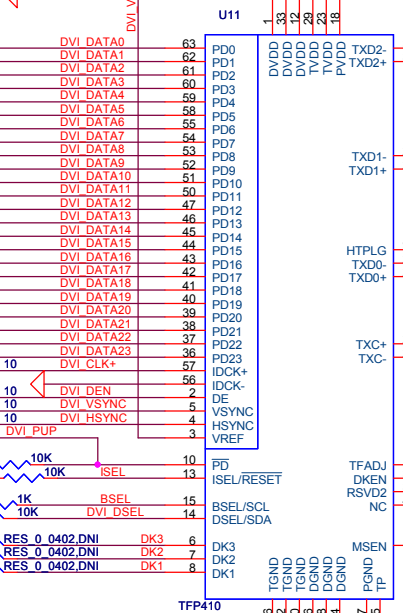
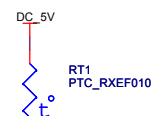
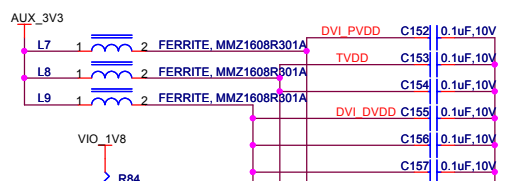
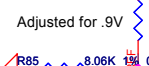
BLUE

GREEN

RED

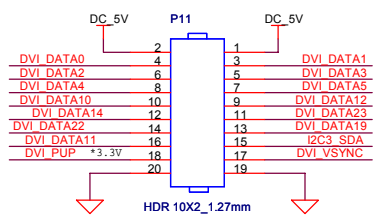


On the processor, there is a shift in the location of DSS0-5 and DSS18-23 that is required in order to run at the maximum frequency on the DSS interface. The naming of the signals take into account this shift. If there is a need to revert back to the standard configuration, remove RP7 and RP2 and install RP1 and RP5.

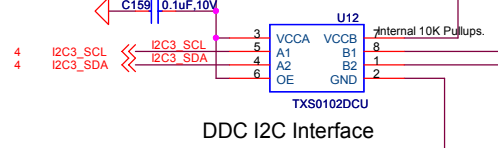
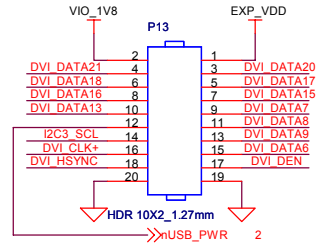


DVI-D Interface

Insures that the DVI-D is powered down at powerup.



LCD RGB Interface



DDC I2C Interface



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